

Improving GCC instruction scheduler for IA64 platform

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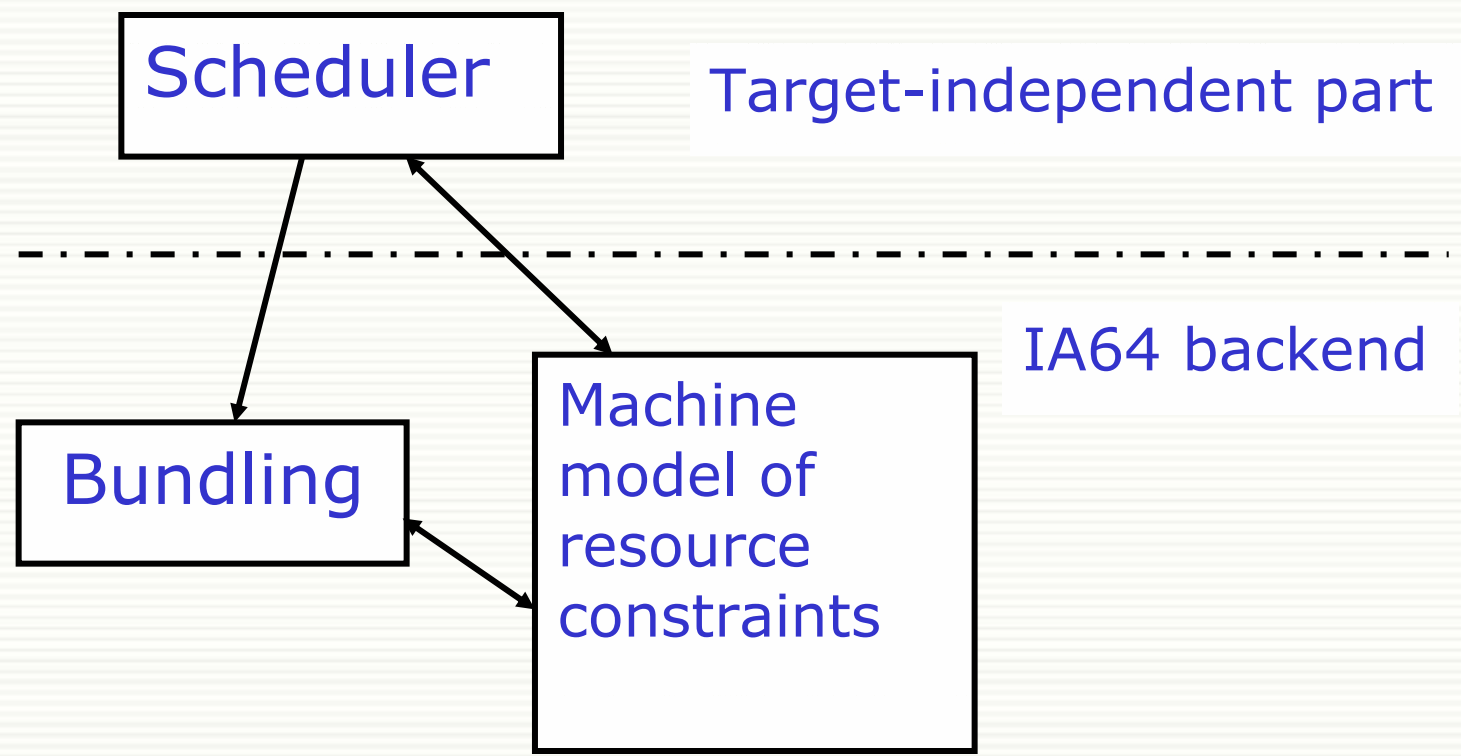
Motivation of our work

- IA64 requires the compiler to explicitly expose instruction-level parallelism
- For this IA64 features control/data speculation, predication, prefetching, rotating registers
- Instruction scheduler is one of the important components of the compiler for achieving this goal

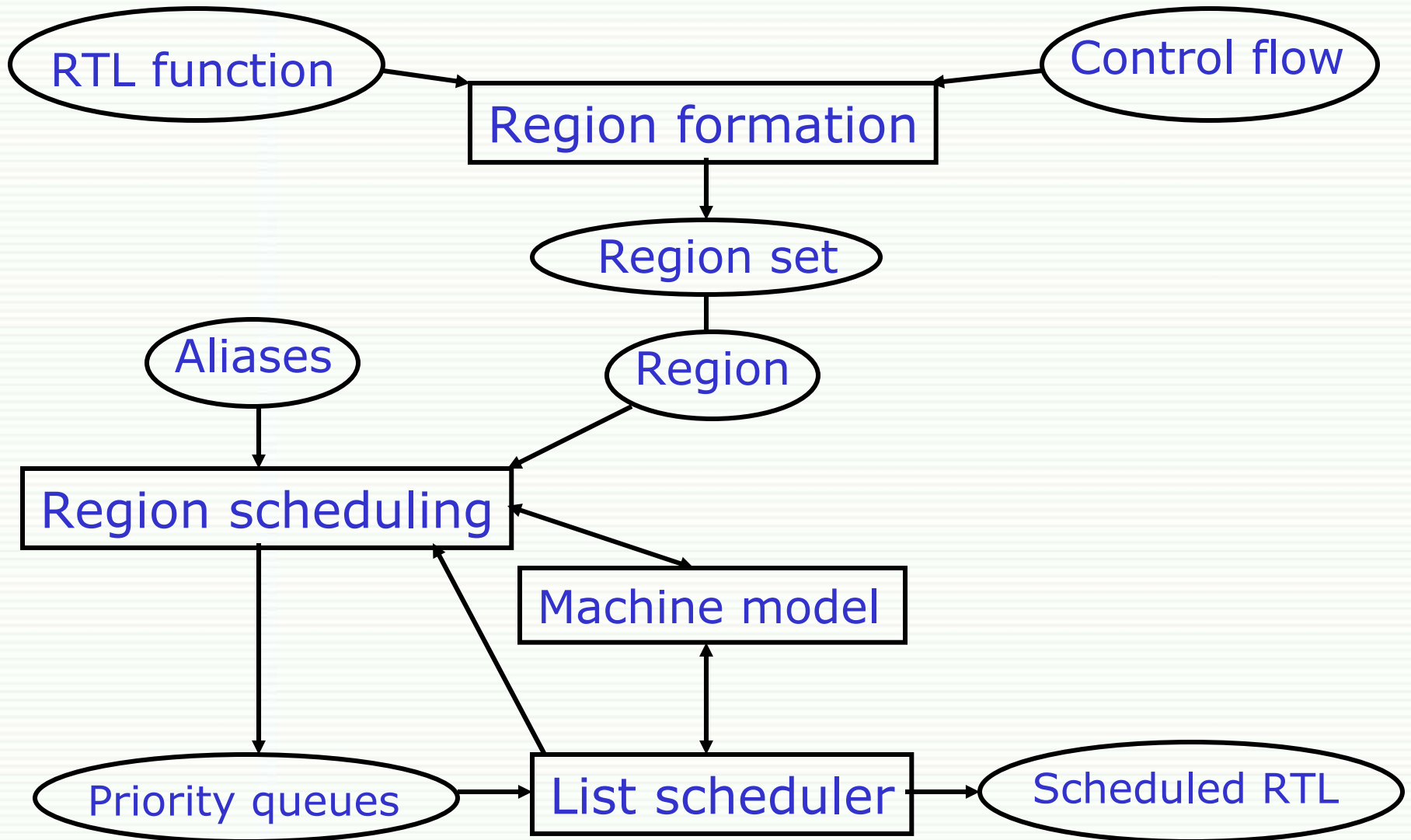
Goals of the project

- Implement control/data speculation support
- Solve alias analysis problem by propagating alias information from TREE level to the scheduler
- Use built-in GCC probability analysis instead of current inaccurate evaluation

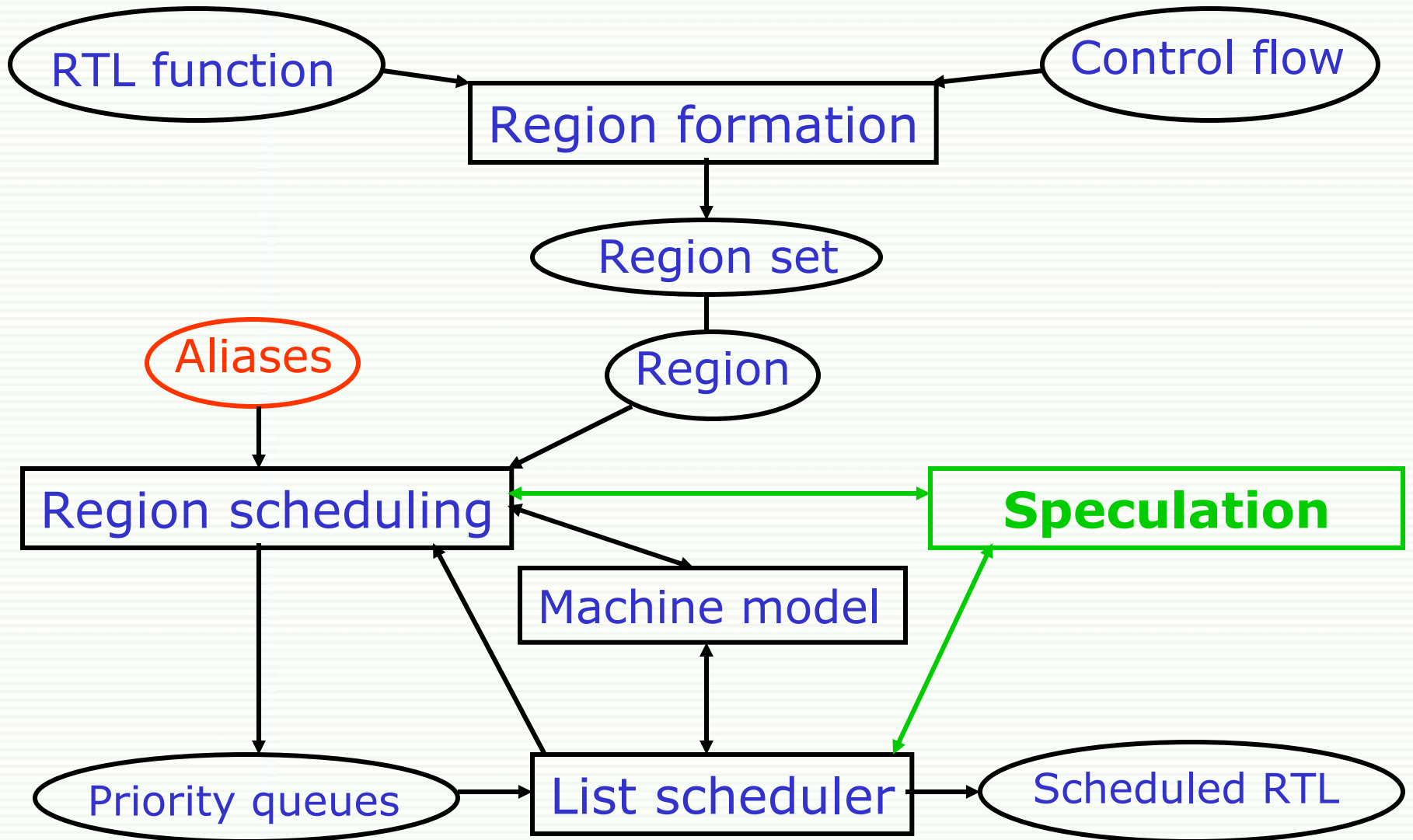
GCC scheduling on IA64



Anatomy of GCC scheduler



Anatomy of GCC scheduler



Current project status

- Patch for using GCC probability information is implemented and tested
- Data speculation patch is designed and is being implemented
- Alias information patch is being designed
 - Sanjiv Gupta's alias patch (which addresses alias analysis problems for architectures without displacement) is fixed for 4.0 and applied to our GCC snapshot for further experiments

Technical summary

- Patches are developed against GCC 4.0 20050110 CVS snapshot
- Patches are tested on ia64-unknown-linux-gnu and i686-pc-linux-gnu architectures
- HP rx2600 servers are used as hardware (*2 systems presented by HP*)
- SPEC CPU2000 is used for benchmarking

Project summary

Project team is:

- Andrey Belevantsev – team leader
- Dmitry Melnik – software engineer
- Maxim Kuvyrkov – software engineer

Consulting of the project is provided by Vladimir Makarov, Red Hat.

Project timeframe is
January 15th – July 15th