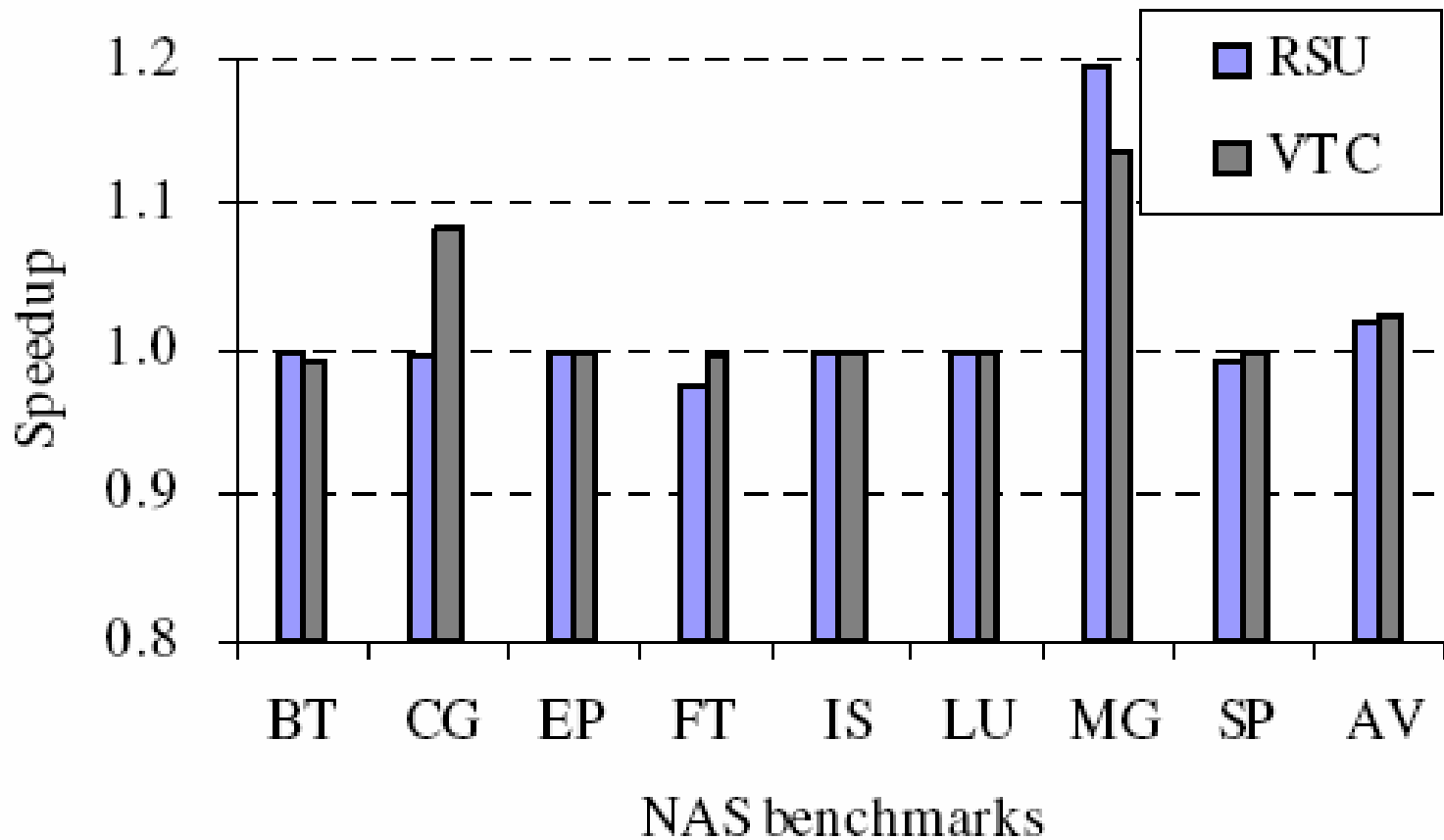


# Optimizing Performance for IA64

Efforts in Tsinghua University

# Current Work

- Code Generation Optimization for ORC
  - Register Allocation
    - Register sensitive unrolling(RSU)
    - Variable Type Conversion (VTC)
      - Rotating registers are more than necessary
      - Static registers are not enough
      - Change post increment variant to loop variant
  - Data Speculation



# Current Work(2)

- OpenMP for ORC
  - GCC front-end extension to support OpenMP directives
  - GCC to WHIRL translation
  - Mapping OpenMP to run time library calls
  - OpenMP Runtime library on IA64

# Funding

- Current
  - Gelato and Intel
- But
  - Intel will not support these efforts any more in 2005, they are more interested in many-core processors
  - Planned work may be supported by Intel
    - Debugging support for OpenMP programs
      - Relative debugging, predicate based technology
    - Dynamic compilation

# Expertise

- Code generation optimization
  - For WHIRL, but could be applied to new GCC
- GCC front-end
- OpenMP related( gomp? )

# Staffs

- 5 faculties
  - Prof. Zheng Weimin( General leader )
  - Prof. Tang Zhizhong( Code generation optimization )
  - Prof. Zhang Suqin( C++ front end )
  - Assoc. Prof. Chen Wenguang( Parallelizing )
  - Assoc Prof. Wang Sheng Yuan( C++ front end)
- More than 15 graduate students

# Possible works in GCC

- Porting some optimization methods in ORC to GCC
  - Improve the current software pipelining implementation in GCC
- OpenMP support for GCC
  - Dual core Itanium this year
  - How about gomp?

Thanks.